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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,468	11/08/2001	Yoshiaki Katayama	214708US2PCT	5104

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,468	KATAYAMA, YOSHIAKI	
	Examiner	Art Unit	
	Nilesh Shah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/08/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are presented for examination.

Claim Rejections - 35 USC § 103

2. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiguchi et al (6,772,419) (hereinafter Sekiguchi) in view Townsley et al (5,623,677) (hereinafter Townsley).

3. As per claim 1, Sekiguchi teaches the invention substantially as claimed including a method which employs a plurality of OSs whose execution is controlled by a processor, wherein said plurality of OSs include:

a primary OS for receiving a timer interrupt issued from a hardware timer after a predetermined time lapse(abstract; col. 2 lines 44-50; col. 23 lines 45-60; col. 24 line 65-col. 25 line 5);

a secondary OS treated as a task to be executed by said primary OS (col. 2 lines 44-50; col. 13 lines 4-20; col. 21 lines 20-34);

upon receiving said timer interrupt, determining whether there exists any task to be executed, this step being performed said primary OS (col. 6 lines 33-50; col. 24 lines 8-16); and

when there exists any task to be executed on said secondary OS, interrupting said secondary OS (col. 24 lines 30-40;col. 6 lines 33-50; col. 24 lines 8-16).

4. Sekiguchi does not teach a power saving processor. Townsley teaches a power saving processor (col. 3 lines 10-24; col. 17 lines 62-67).

5. It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Sekiguchi and Townsley because Townsley's method of power saving would improve Sekiguchi's system by reducing power used when the processor is not being used.

6. As per claim 2, Sekiguchi teaches which employs a plurality of OSs whose execution is controlled by a processor,

operation of said processor being stopped when there exists no task to be executed on said plurality of OSs (col. 6 lines 33-50; col. 24 lines 8-16);

method controlling timer interrupt processing performed by a hardware timer which activates said processor after an arbitrary time lapse (col. 18 lines 28-40; col. 24 lines 30-40);

a primary OS for receiving a timer interrupt issued from said hardware timer and a secondary OS treated as a task to be executed by said primary OS (col. 6 lines 33-56; col. col. 7 lines 1-15);,

method comprises a primary-os process step performed by said primary OS, a secondary-os process step performed by said secondary OS, and a secondary-os interrupt step, said primary-os process step including (col. 24 lines 30-40):

a step of detecting said timer interrupt (col. 24 lines 30-40);

a first determination step of, upon receiving said timer interrupt, determining whether there exists any task to be executed (col. 6 lines 33-50; col. 24 lines 8-16); and

a processor stopping step of, when there is no task to be executed, stopping said processor (col. 24 line 65- col. 25 line 5);

said secondary-os process step including:

a second determination step of determining whether there exists any task to be executed (col. 24 lines 30-40); and

a step of, when there is no task to be executed, handing over processing to said first determination step (col. 24 line 65- col. 25 line 5);

whereby when said first determination step has determined that there exists any task to be executed on said secondary OS, said secondary-os interrupt stepperforms interrupt processing on said secondary OS, and executes said second determination step at a predetermined time measured from said interrupt (abstract; col. 2 lines 44-50; col. 23 lines 45-60; col. 24 line 65- col. 25 line 5).

Townsley teaches a power saving processor (col. 3 lines 10-24; col. 17 lines 62-67).

7. As per claim 3, Sekiguchi teaches a method wherein said secondary-os interrupt step is executed by a periodically-activating handler which interrupts said secondary OS at regular time intervals (col. 12 lines 52-60; col. 6 lines 33-50)

8. As per claim 4, Sekiguchi teaches a method wherein said secondary-os interrupt step is executed by an alarm handler which interrupts said secondary OS after a specified time period (col. 18 lines 28-40; col. 24 lines 30-40).

9. As per claim 5, Sekiguchi teaches a method wherein said secondary-os interrupt step is executed by a high-priority task which is a task for interrupting said secondary OS and has a highest priority order among tasks to be executed by said primary OS (col. 7 lines 1-14).

10. As per claim 6, Sekiguchi teaches a method wherein said processor stopping step includes a step of determining whether time taken until said hardware timer issues a next timer interrupt is longer than a predetermined time, and if a measured time is longer than said predetermined time, said processor stopping step stops operation or said processor(col. 18 lines 28-40; col. 24 lines 30-40).

11. As per claim 7, Sekiguchi teaches a method wherein said primary-os process step further comprises steps of: when said hardware timer periodically performs timer interrupt processing at regular time intervals, determining whether timer interrupt processing is

required again by a time at which a task is to be executed(col. 2 lines 44-50; col. 13 lines 4-20; col. 21 lines 20-34); and

if timer interrupt processing is not required again, stopping said hardware timer(col. 18 lines 28-40; col. 24 lines 30-40).

12. As per claim 8, Sekiguchi teaches a method wherein said primary-os process step further comprises a step of:

detecting a timer interrupt issued by a long-periodic hardware timer which issues a timer interrupt at a time interval longer than that of said hardware timer (col. 18 lines 28-40; col. 24 lines 30-40).

13. As per claim 9, Sekiguchi teaches a method wherein said primary-os process step further comprises a step of:

detecting a timer interrupt issued by a time-of-day timer which measures a time of day as well as issuing a timer interrupt at a predetermined time or day (col. 18 lines 28-40; col. 24 lines 30-40).

14. Claim 10 is rejected based on the same rejection as claim 2 above.

15. Claim 11 is rejected based on the same rejection as claims 1 and 2 above.

16. Claims 12-13 are rejected based on the same rejection as claim 8-9 above.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2195

NS
March 31,2005

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2